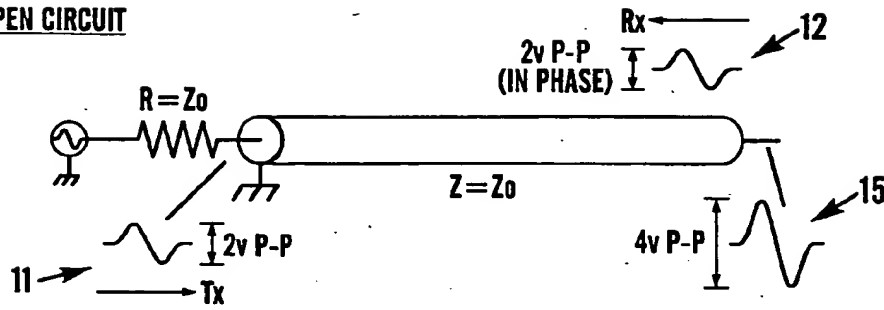
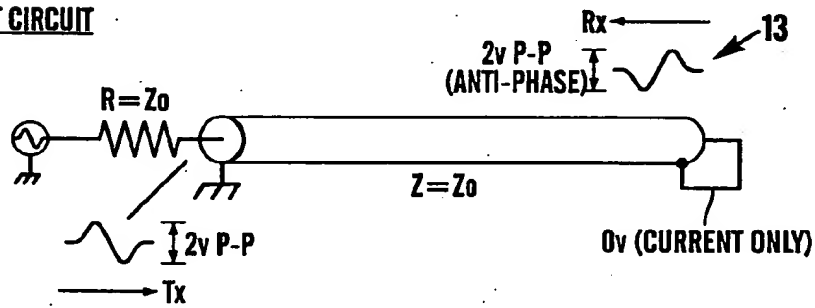


**OPEN CIRCUIT****SHORT CIRCUIT****Fig. 1**

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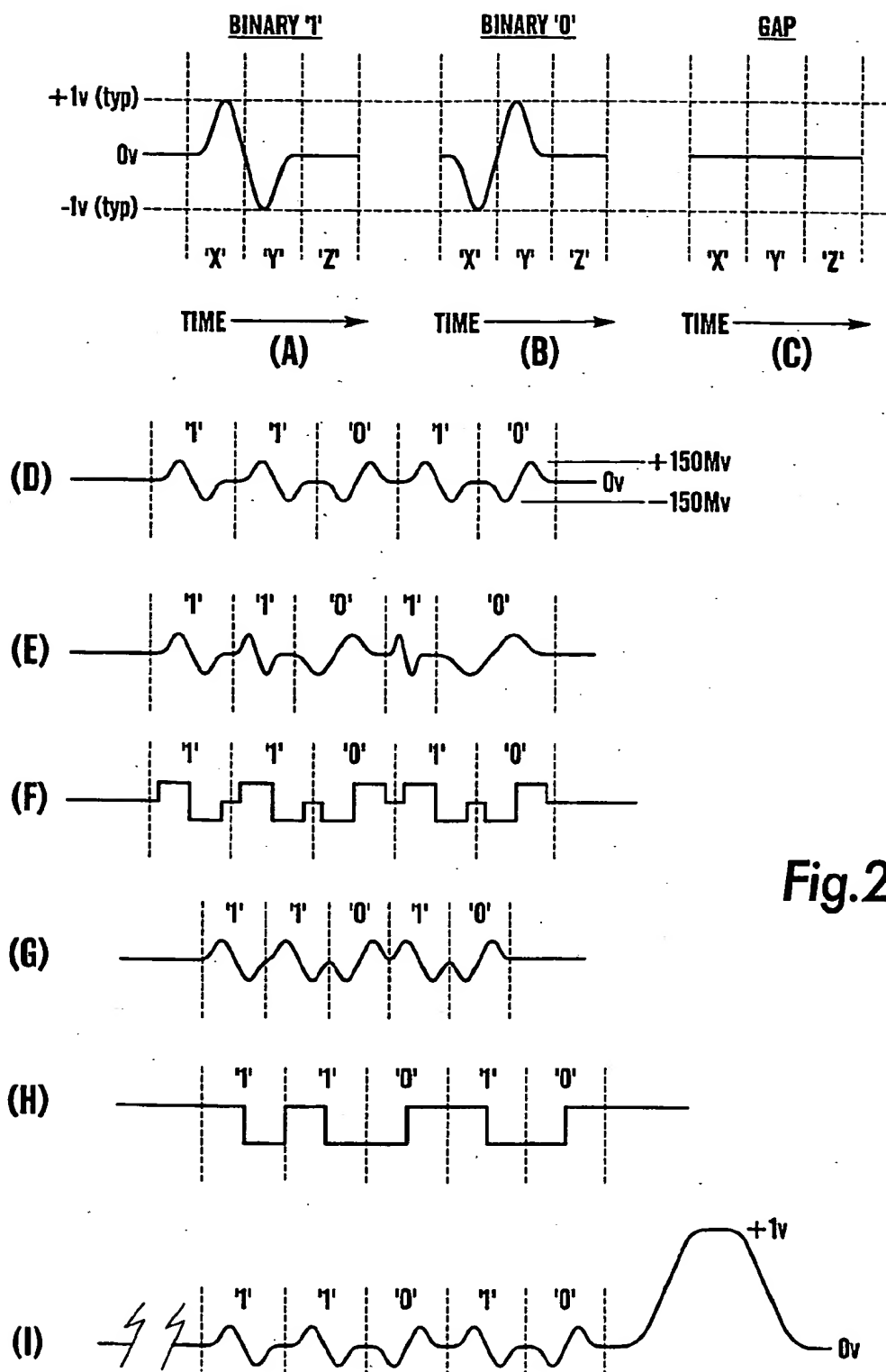


Fig.2

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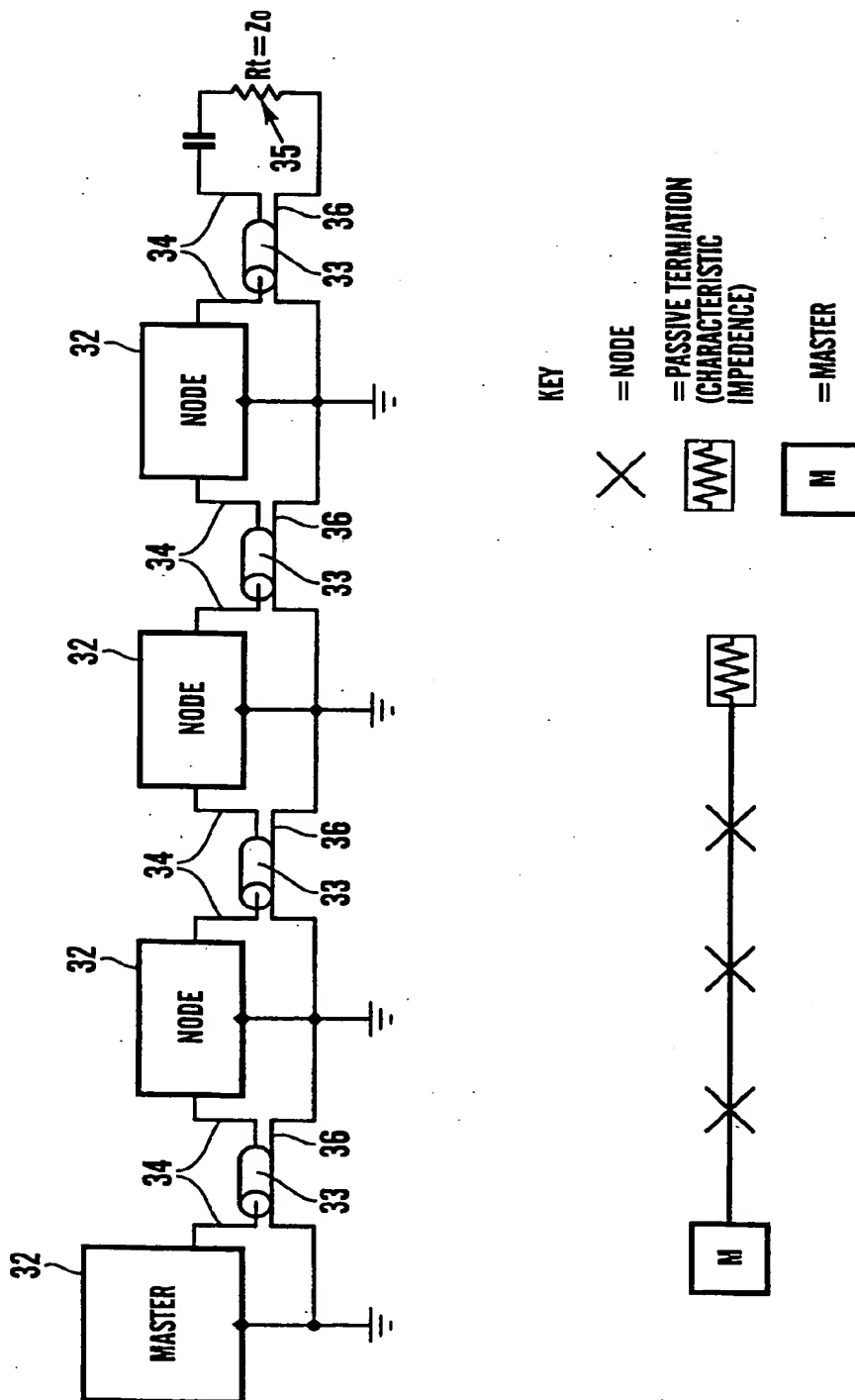


Fig.3



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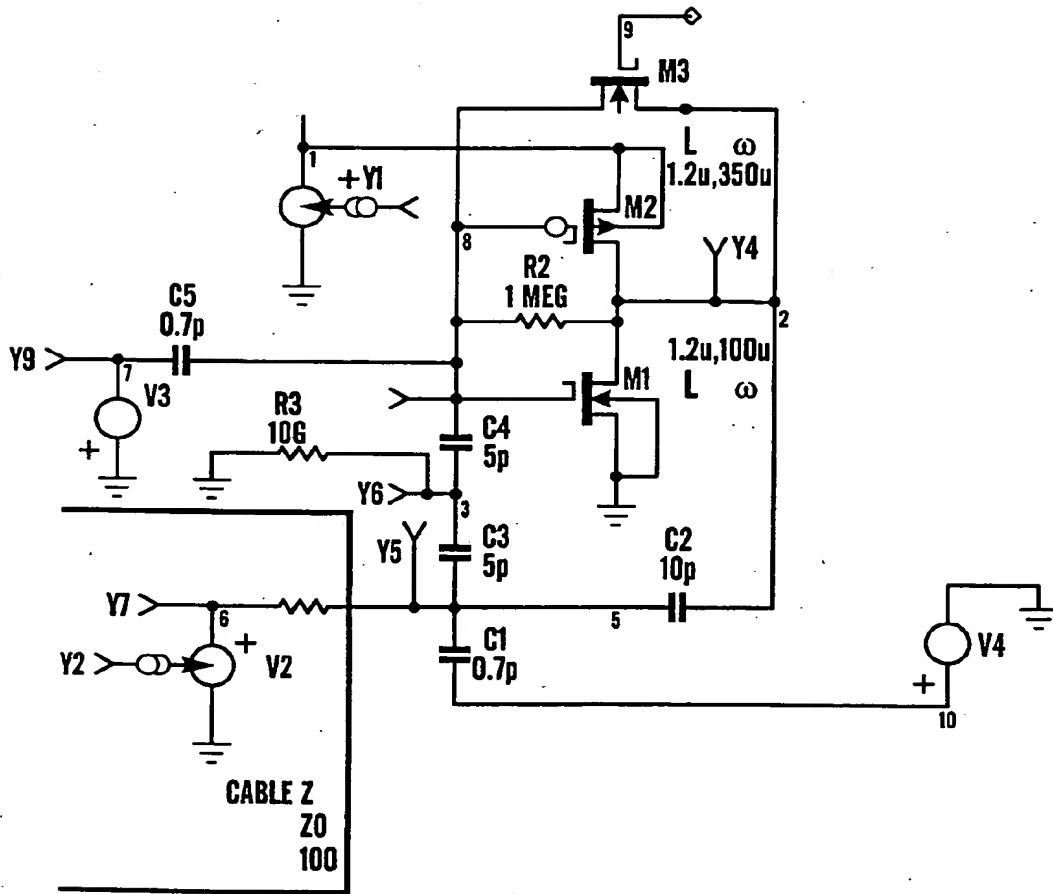


Fig.4A

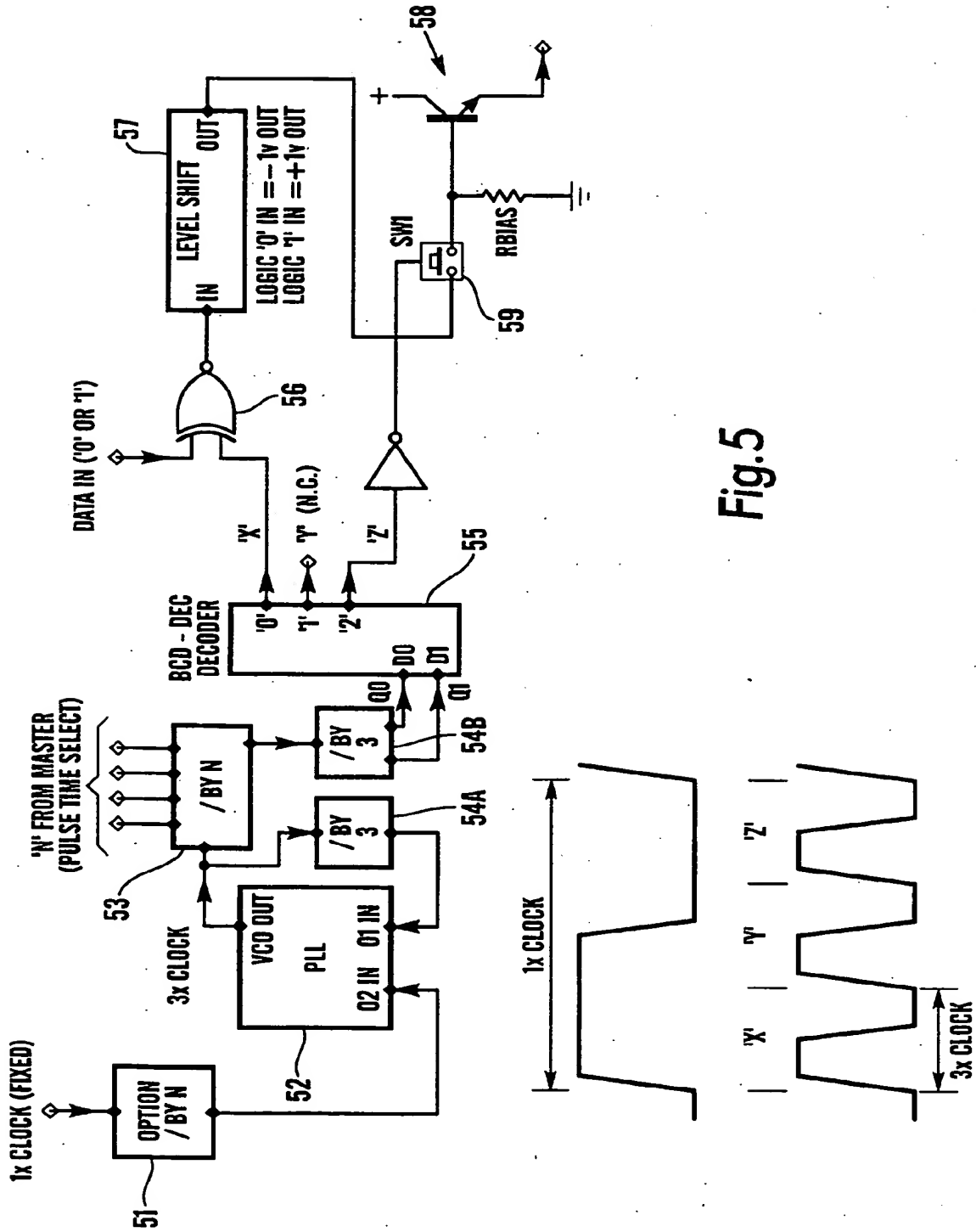


Fig.5

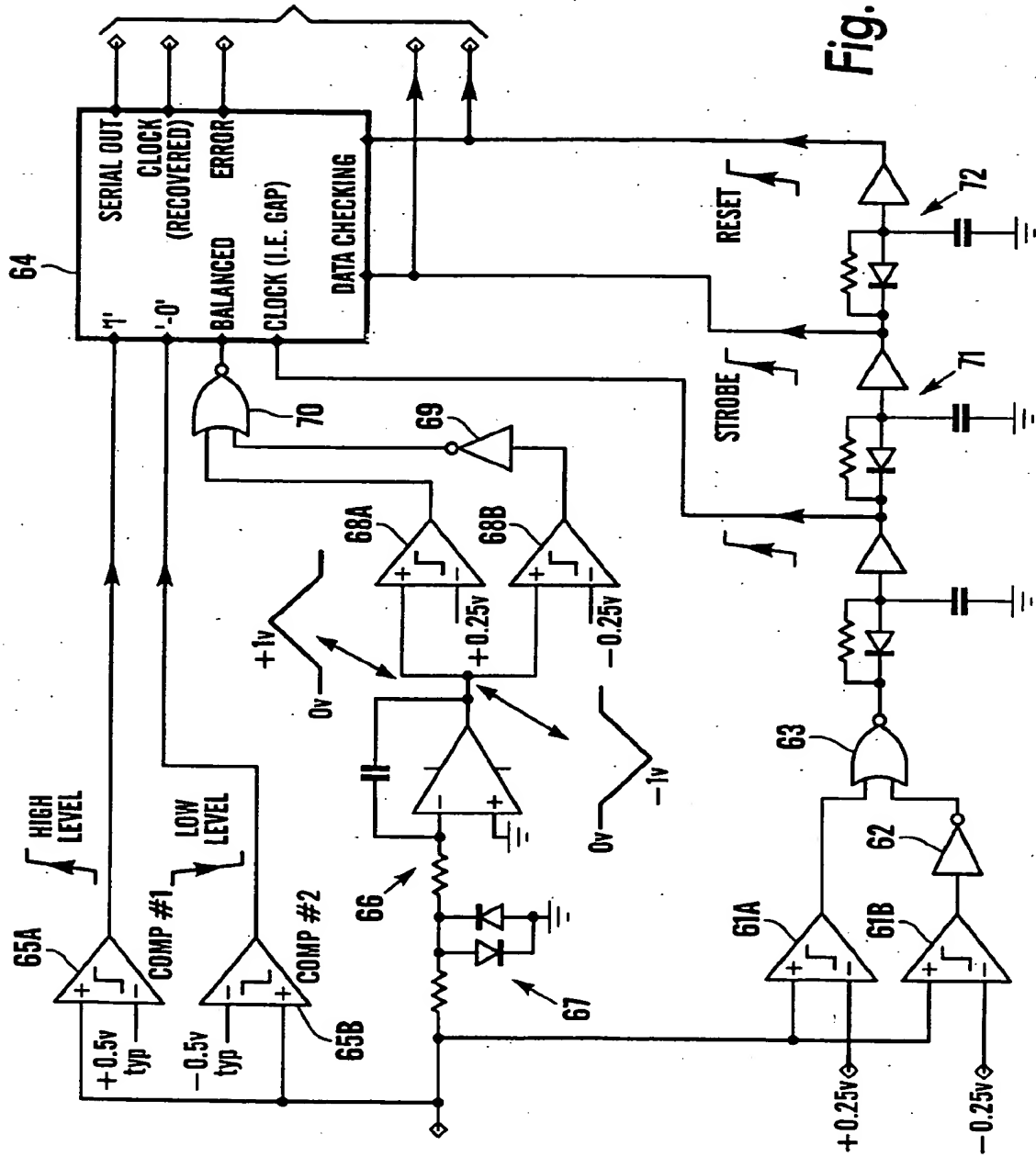


Fig. 6

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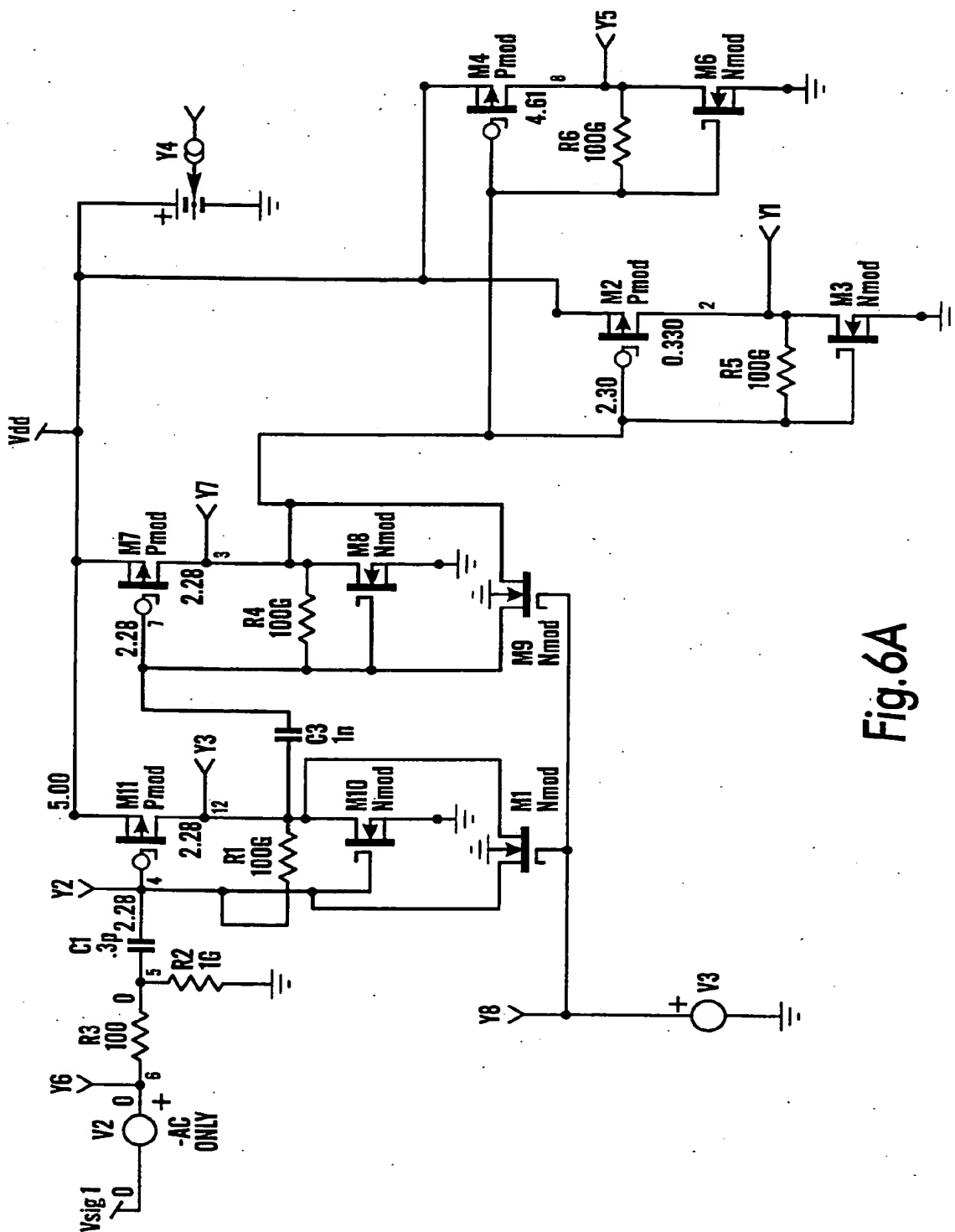


Fig. 6A

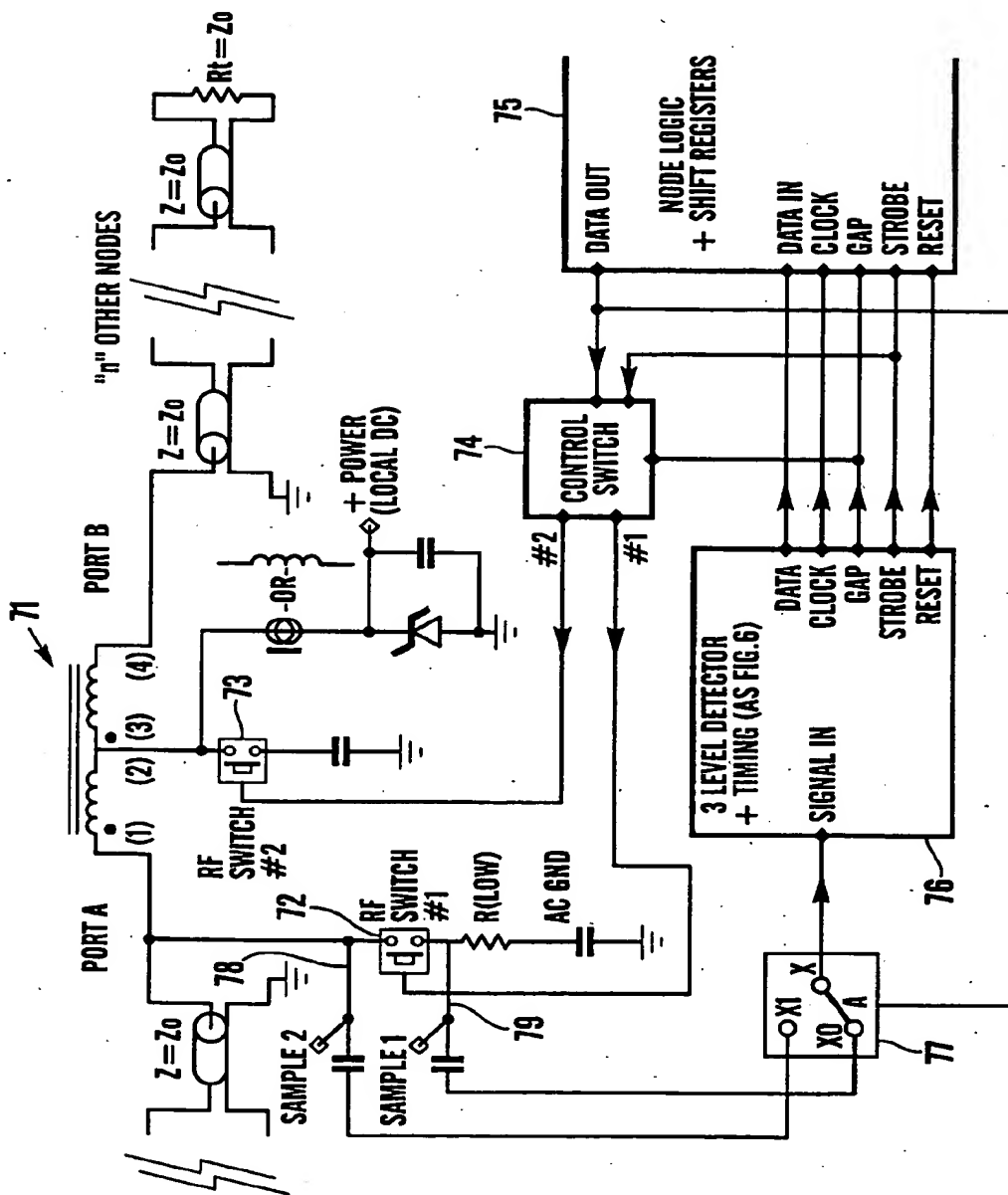


Fig.7

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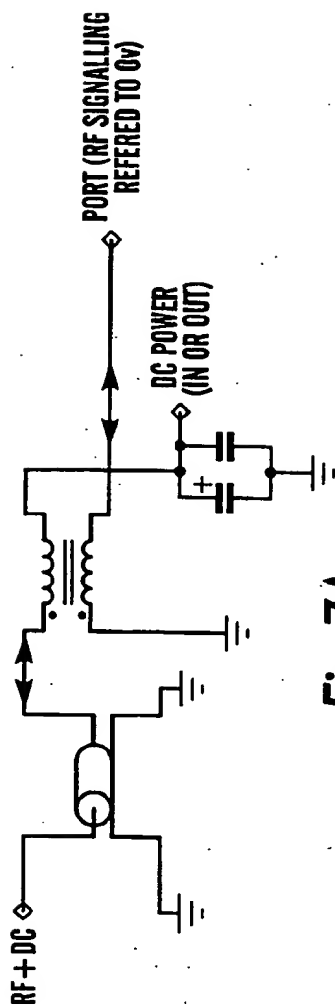


Fig.7A

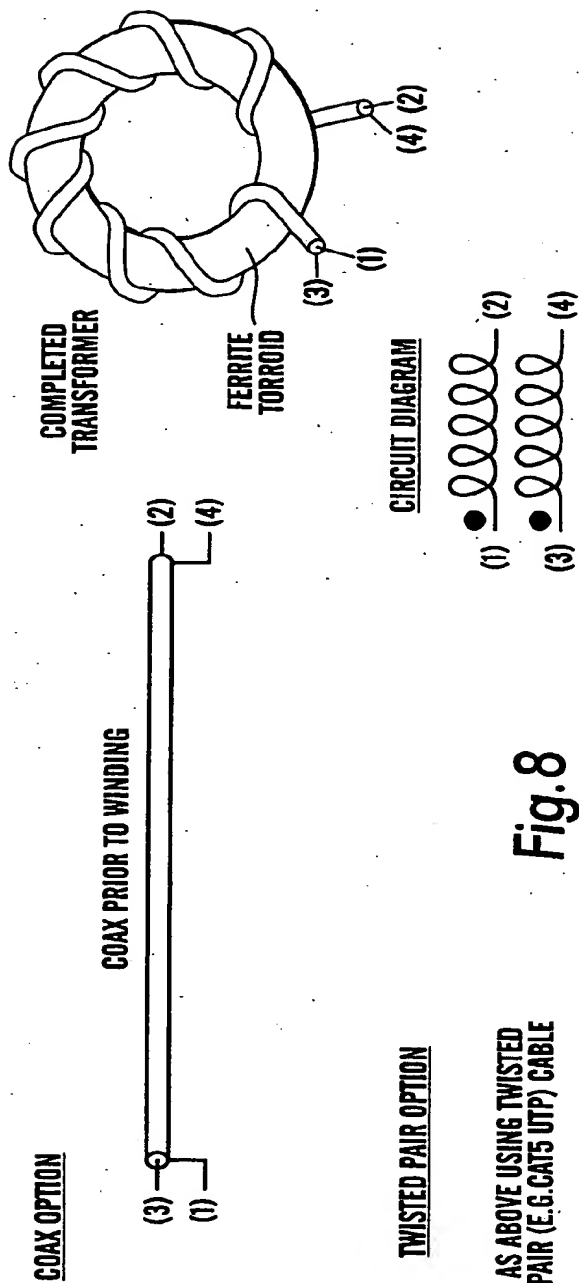


Fig.8

AS ABOVE USING TWISTED PAIR (E.G. CAT5 UTP) CABLE

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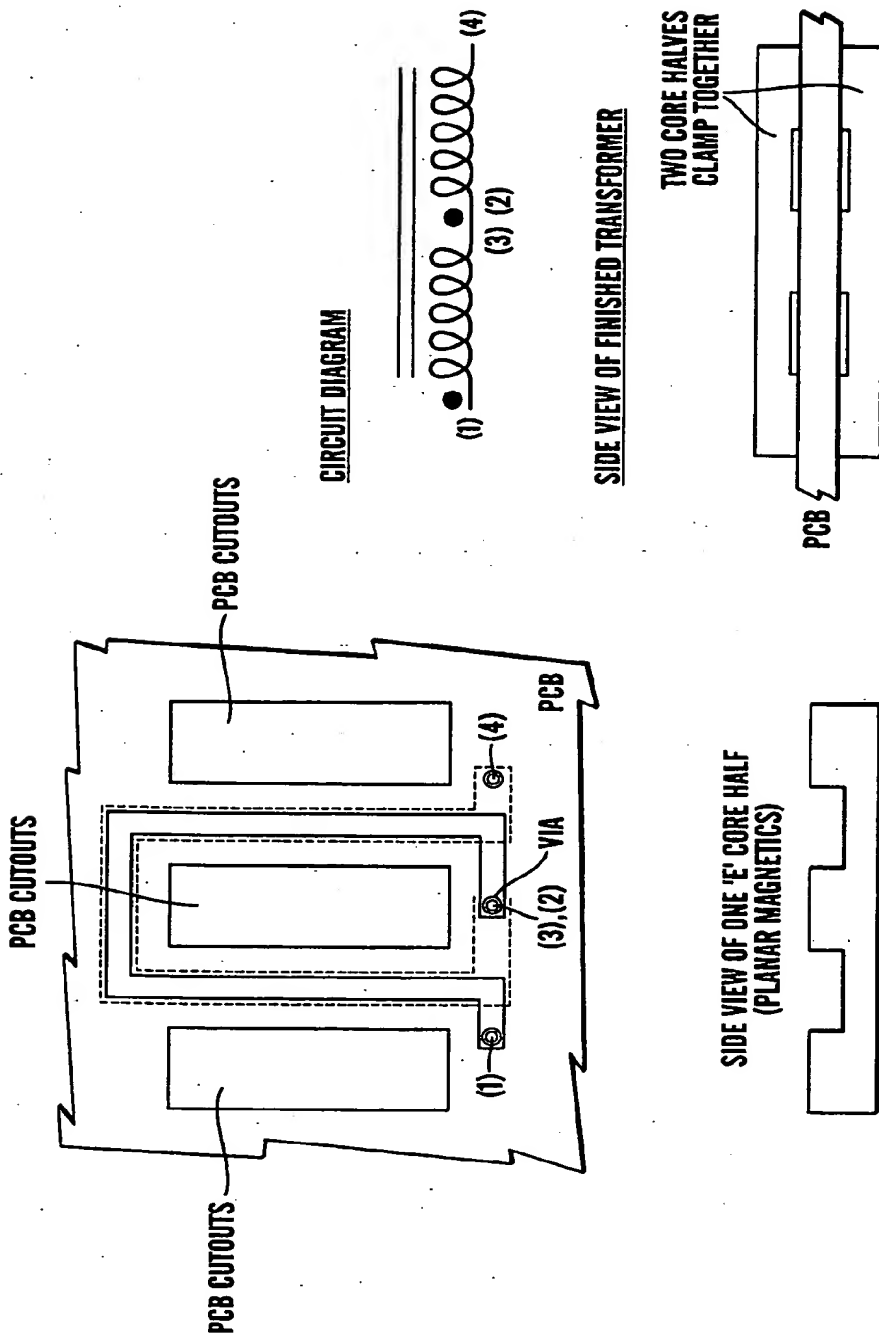


Fig.9

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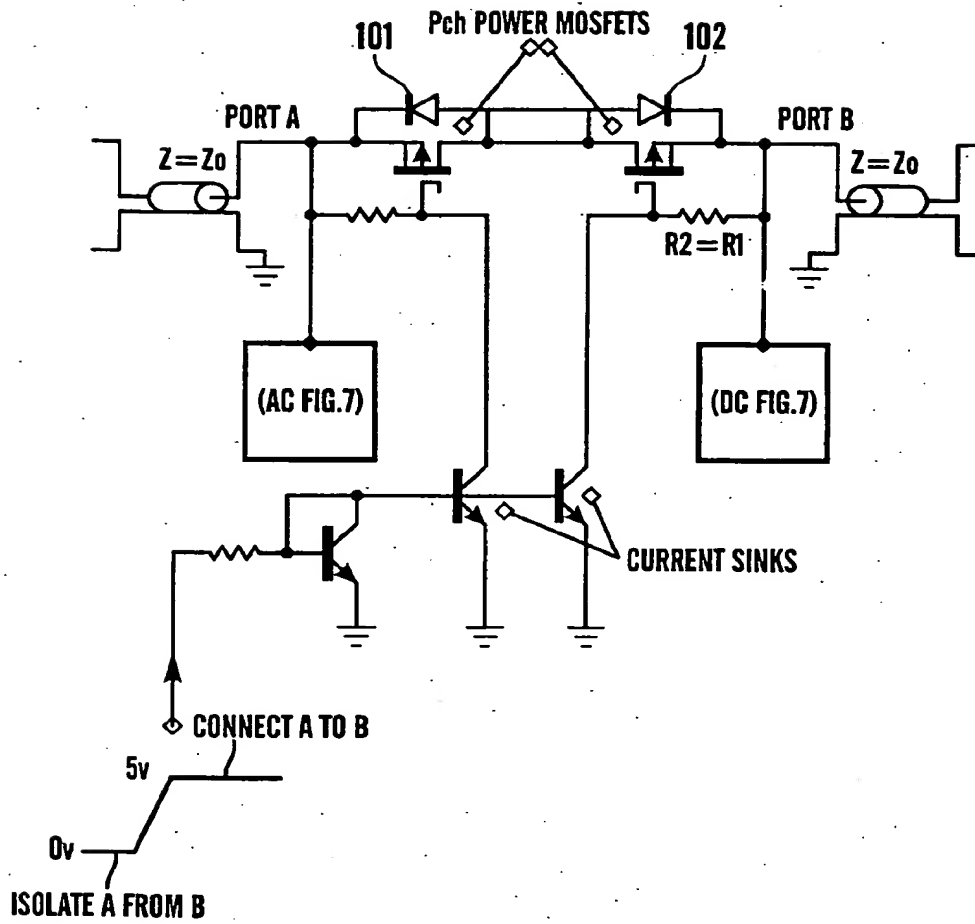


Fig.10

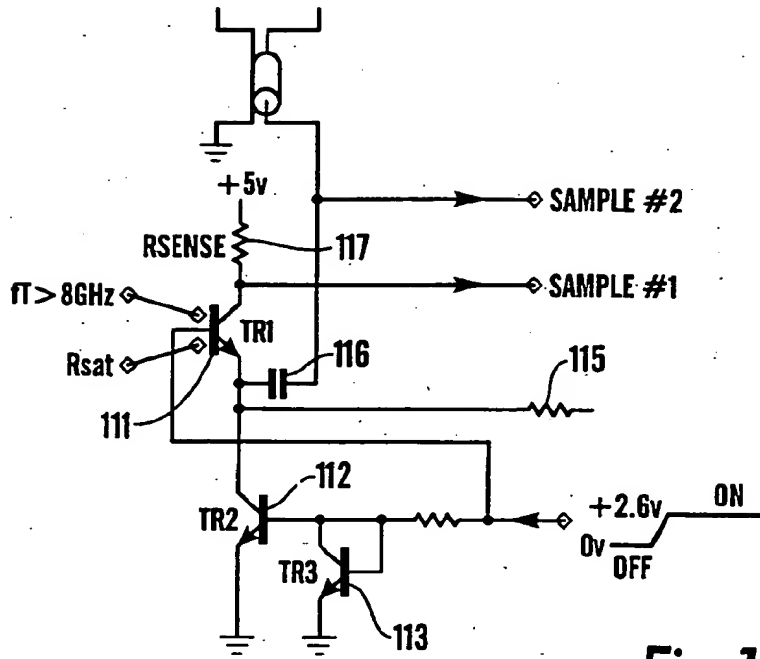


Fig. 11

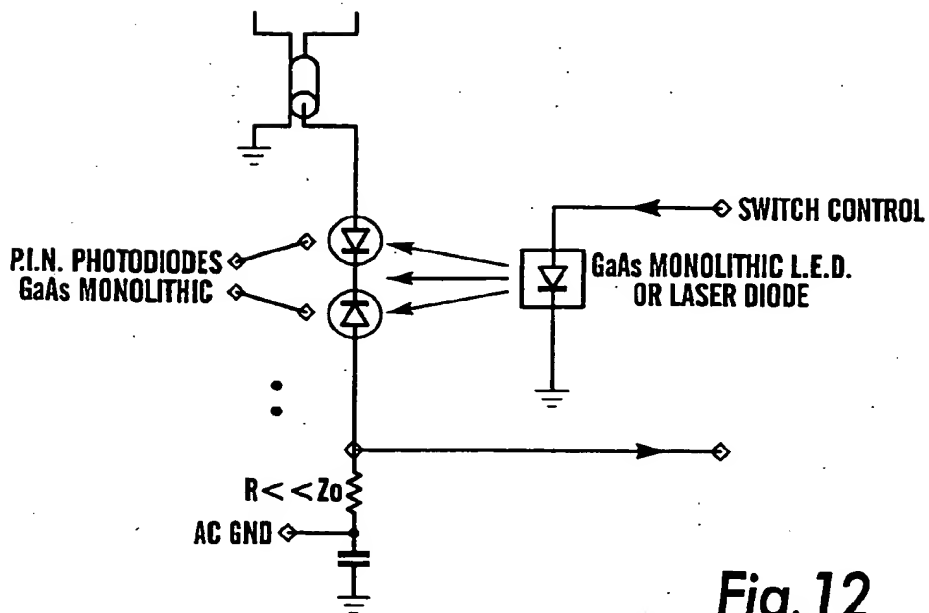
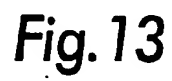
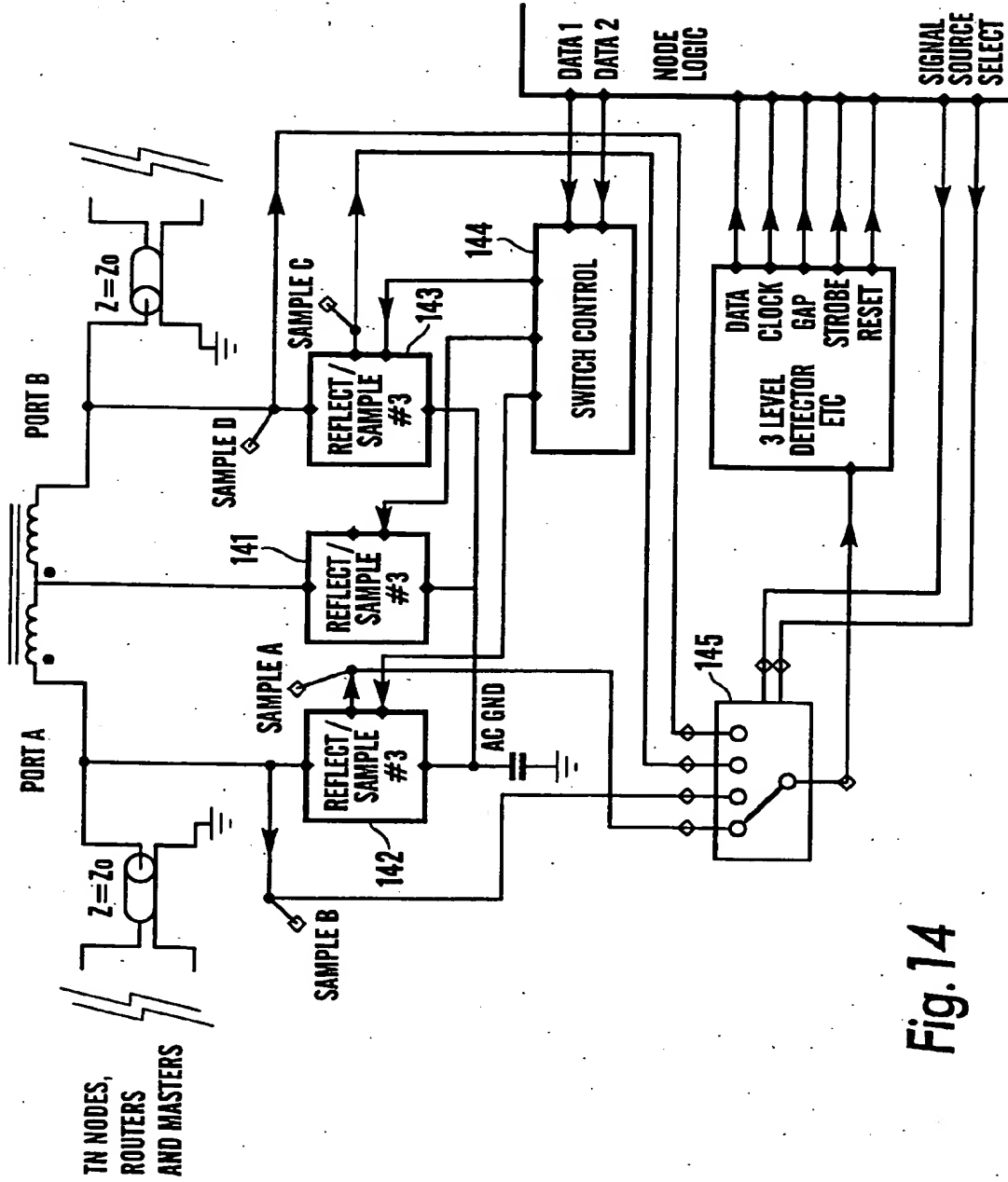


Fig. 12





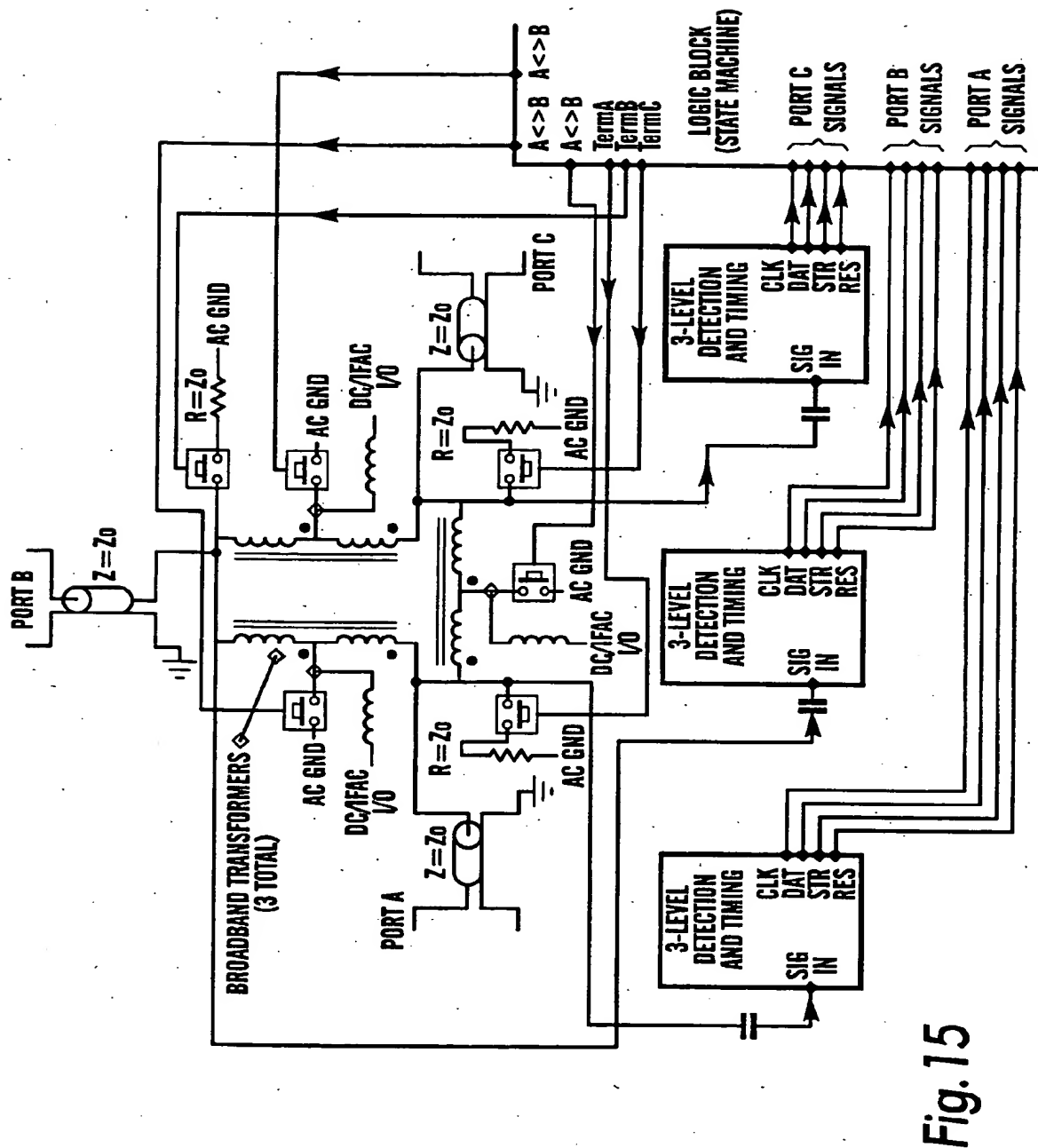


Fig. 15

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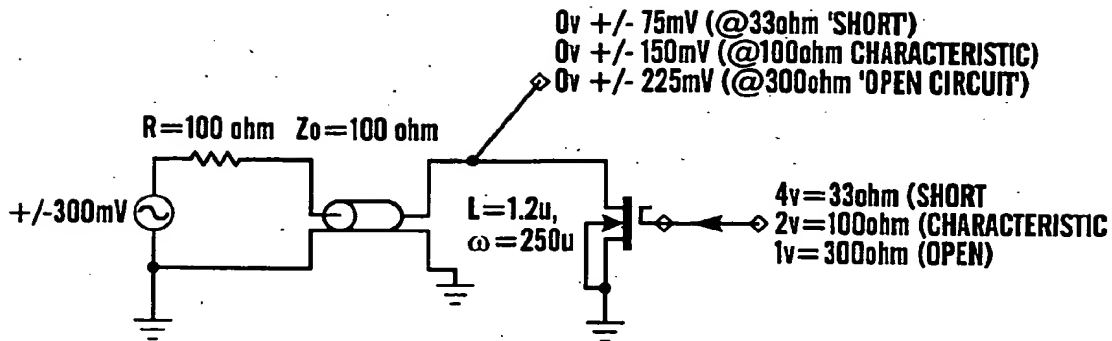


Fig. 15A

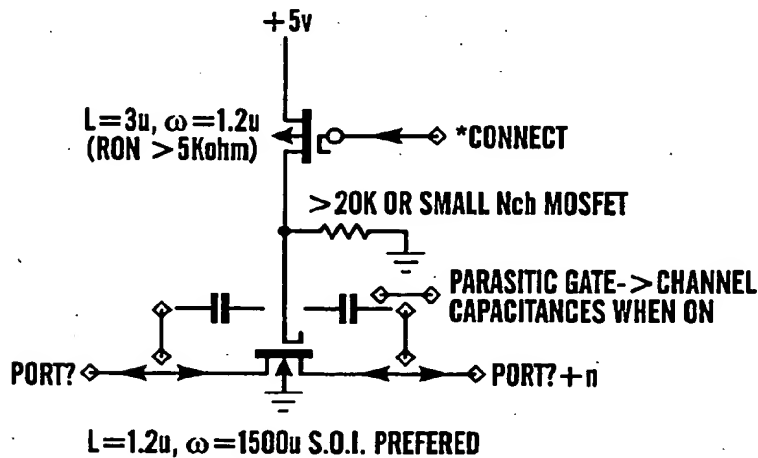


Fig. 15B

000720" 00000000

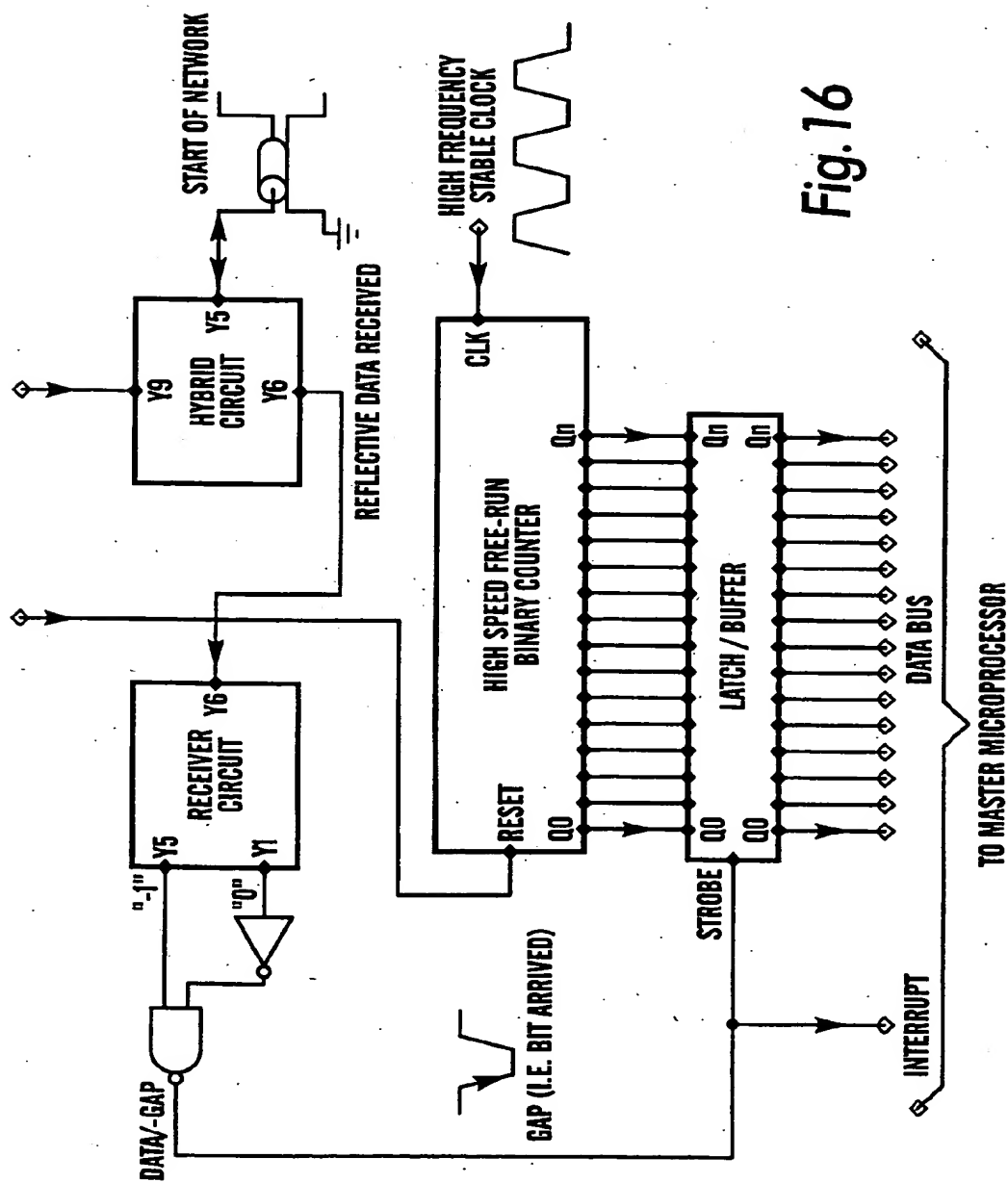
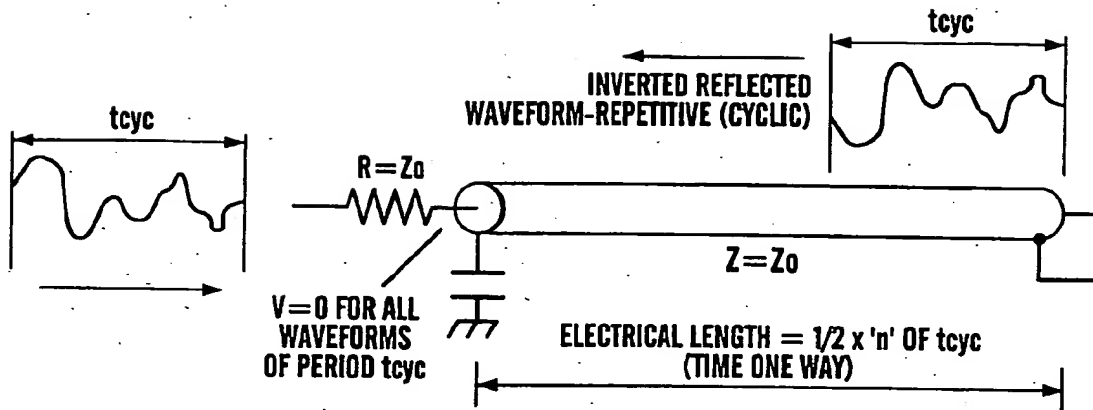


Fig. 16



MEMORY EFFECT ON WANTED SIGNALS WHEN THEN COMBINED AT THE COAX ENTRANCE  
(SPURIOUS SIGNALS HAVING BEEN MOVED)

$$\begin{array}{ccccc}
 \text{WAVEFORM 1} & + & \text{WAVEFORM 2} & = & \text{WAVEFORM 3} \\
 \text{(INCOMING SIGNAL)} & & \text{(RETURNING SIGNAL)} & & \text{(RESULT)} \\
 \text{WAVEFORM 4} & + & \text{WAVEFORM 5} & = & \text{WAVEFORM 6}
 \end{array}$$

$$\begin{array}{ccccc}
 \text{WAVEFORM 7} & + & \text{WAVEFORM 8} & = & \text{WAVEFORM 9} \\
 \text{(INCOMING SIGNAL)} & & \text{(RETURNING SIGNAL)} & & \text{(RESULT)} \\
 \text{WAVEFORM 10} & + & \text{WAVEFORM 11} & = & \text{WAVEFORM 12}
 \end{array}$$

Fig. 17

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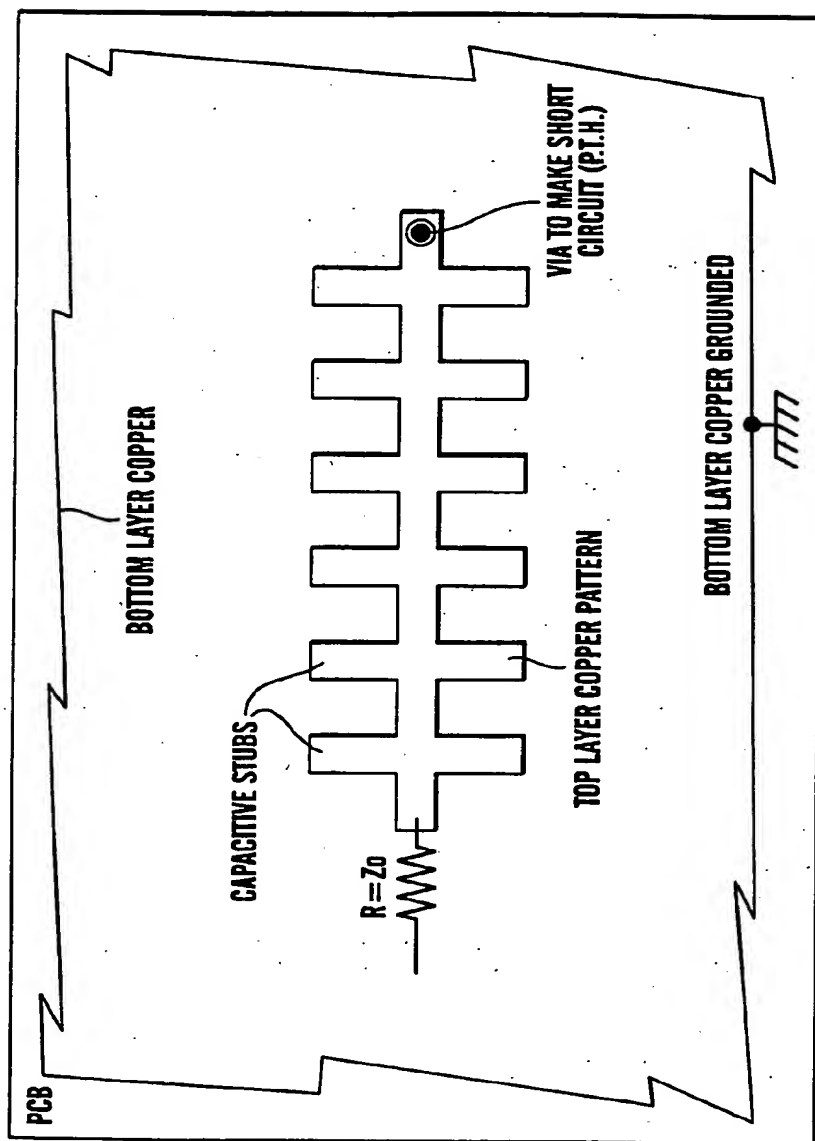


Fig.18